REMARKS

Claims 1-21 are pending in this application. The objections and rejections set forth in the Office Action are respectfully traversed below

The Drawings:

The Office Action objected to Figures 1 - 16 of the drawings for allegedly not labeling the boxes shown therein. It is submitted that this objection is improper and should be withdrawn because there are no "boxes" shown in Figures 1 - 16. As explained in the Specification, these drawings provide sectional/perspective views of a semiconductor laser device according the preferred embodiments of the present invention. There is no need to provide any "labels" for any "boxes."

The Prior Art Rejections:

Claims 1 - 2, 4, 6, 8 - 9, 11, and 19 - 20 were rejected under 35 U.S.C. §102 over **Ikeda, et al.** (USP 5,956,361). Claims 5, 10, 16 and 21 were rejected under 35 U.S.C. §103 over **Ikeda**, in view of **Tanaka, et al.** (USP 6,298,079). Claims 3, 7, 12 and 17 - 18 were rejected under 35 U.S.C. §103 over **Ikeda**, in view of **Yamamoto, et al.** (USP 6,064,079). Claims 13 - 15 were rejected under 35 U.S.C. §103 over **Ikeda**, in view of **Yamamoto**, and further in view of **Ishikawa, et al.** (USP 6,118,801).

First, it should be noted that the rejection of claims 4 and 6 under 35 U.S.C. §102 are improper because the Examiner relied upon the combination of **Ikeda** and **Yamamoto** for claim 3 and the combination of **Ikeda** and **Tanaka** for claim 5. Since claim 4 depends from claim 3 and claim 6 depends from claim 5, claims 4 and 6 cannot be rejected by **Ikeda** alone. Therefore, the rejection of claims 4 and 6 under 35 U.S.C. §102 are improper and should be withdrawn. For the purposes of this response, the rejection of claims 4 and 6 will be considered under 35 U.S.C. §103, as an extension of the rejections of their base claims 3 and 5.

It is submitted that the present claimed invention patentably distinguishes over the prior art for at least the reasons that nothing in the cited prior art, either alone or in combination, teaches or suggests "said second semiconductor layer including a cladding layer which comprises a lower layer having a first width at its lower end and an upper layer having a second width larger than said first width at its lower end, both of said lower layer and said upper layer having a larger band-gap than that of said active layer" (independent claim 1), nor "the step of forming said second semiconductor layer comprising the step of forming a cladding layer which comprises a lower layer having a first width at its lower end and an upper layer having a second width larger than said first width at its lower end, both of said lower layer and said upper layer having a larger band-gap than that of said active layer" (independent claim 11).

The prior art rejections set forth in the Office Action rely upon the primary reference to **Ikeda** for allegedly disclosing all the features recited in independent claims 1 and 11. The Office Action referred to the various layers disclosed in **Ikeda**, without identifying the specific correspondence

between these layers and the specific claimed features of independent claims 1 and 11. Nevertheless, even without the Examiner's specific discussion of how the structures of **Ikeda** correspond to the claimed features, it is noted that none of the features disclosed in **Ikeda** teaches or suggests the details of the upper and lower layers of a cladding layer in the second semiconductor layer, as specifically recited in independent claims 1 and 11, as identified above.

If the Examiner intended to assert that the second upper cladding layer 107 of **Ikeda** corresponds to the present claimed upper layer, then it would be clear that **Ikeda** ***teaches away*** from the present claimed invention specifically reciting the width of the lower end of the upper layer of the cladding layer to be larger than the width at the lower end of the lower layer of said cladding layer. As clearly shown in figure 1 of **Ikeda**, the second upper cladding layer 107 has a continuously ***reducing*** width from its lower end to its upper end. There is never any "second width" that is ***larger*** than a first width, as recited in the present claimed invention. In addition, there is no clear upper and lower layers in the second upper cladding layer 107 in **Ikeda**. For at least these reasons, the present claimed invention patentably distinguishes over the prior art.

If the Examiner intended to assert that the cap layer 108 of **Ikeda** corresponds to the present claimed upper layer, then it would also be clear that the cited prior art does not teach or suggest all the features recited in the present claimed invention. In particular, the cap layer 108 is not a cladding layer as recited in the present claimed invention, as amended. **Ikeda**'s cap layer 108 is comprised of GaAs and has a ***similar*** band gap as that of the active layer 104 composed of Al GaAs. The semiconductor laser described in **Ikeda** has no second semiconductor layer including a cladding

layer which comprises a lower layer and an upper layer, both having a ***larger*** band gap than that of the active layer, as recited in claims 1 and 11 of the present application. For at least these reasons, the present claimed invention patentably distinguishes over the prior art.

Nothing in the further references to **Tanaka**, **Yamamoto**, and **Ishikawa** remedies the deficiencies in the primary reference to **Ikeda**. Indeed, the Examiner relies upon the further references to each of **Tanaka**, **Yamamoto**, and **Ishikawa** for additional features recited in various dependent claims of the present application. While the dependent claims recite further features that are not taught or suggested by any of **Ikeda**, **Tanaka**, **Yamamoto**, and **Ishikawa**, the present claimed invention patentably distinguishes over the prior art, either alone or in combination, for at least the reasons discussed above with regard to **Ikeda**.

In view of the aforementioned amendments and accompanying remarks, the claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

John P. Kong
Attorney for Applicant
Reg. No. 40,054

JPK/kal
Atty. Docket No. **000350**
Suite 1000, 1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

23850
PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made

H:\HOME\JPK\Prosecution\000350\Filings\1.111 Amendment - January 2003

VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/532,791

IN THE CLAIMS:

Claims 1 and 11 have been AMENDED to read as follows:

1. (Amended) A semiconductor laser device comprising:

a first semiconductor layer including an active layer;

a striped second semiconductor layer formed on said first semiconductor layer; and

a current blocking layer formed on said first semiconductor layer on both sides of said second semiconductor layer,

said second semiconductor layer including a cladding layer which comprises a lower layer having a first width at its lower end and an upper layer having a second width larger than said first width at its lower end [and has], both of said lower layer and said upper layer having a larger band-gap than that of said active layer.

11. (Amended) A method of fabricating a semiconductor laser device, comprising the steps of:

forming a first semiconductor layer including an active layer; and

forming a striped second semiconductor layer on said first semiconductor layer, and forming a current blocking layer on said first semiconductor layer on both sides of said semiconductor layer,

the step of forming said second semiconductor layer comprising the step of forming a cladding layer which comprises a lower layer having a first width at its lower end and an upper

layer having a second width larger than said first width at its lower end [and has], both of said lower layer and said upper layer having a larger band-gap than that of said active layer.